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Exploration and Analysis of Transistor Architectures and Their Electrical Characteristics

by

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DECLARATION

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ABSTRACT

This paper looks at the electrical properties of transistor architectures, and particularly the conversion between long-channel and short-channel designs. The initial intervention is the performance analysis of long-channel MOSFETs and verification of their electrical characteristics with respect to the theoretical foundations.

With the further reduction of the scale of devices, short-channel effects, such as hot carrier injection, charging of oxides, and velocity saturation, begin to appear. They are assessed critically and compared with the theoretical expectations to establish their influence on the performance and reliability of devices.

To address the disadvantages of aggressive scaling, more sophisticated device architectures, such as the double-gate MOSFETs and silicon-on-insulator (SOI) technology, FINFETs are put into consideration. The structures also have enhanced control of electrostatics, reduced leakage, and general enhanced performance, and will thus have potential in future nanoscale applications.

The other dimension under consideration in the research is the effect of the critical parameters of design (channel length, gate oxide thickness, and substrate doping) on the threshold voltage and overall device behavior. This question highlights the performance constraints of the traditional transistors and how architectural innovation is the solution to the continuation of the Moore Law, allowing useful transistor operation in the nanoscale.

ACKNOWLEDGEMENT

It is because of the invaluable assistance, advice, and guidance that I would not have managed to complete this project. encouragement which many of you afforded me in the same process. I would like to acknowledge all my helpers. in the successful completion of this thesis.

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1. INTRODUCTION

This Chapter explains the background and rationale of the research undertaken in this thesis. It describes the significance of Transistor scaling in semiconductor technology, critical issues involved in scaling down devices, cites the challenges that face miniaturization, and identifies the role of simulation tools in investigating the electrical characteristics and, finally, the nature of the problem to be solved. Lastly, the chapter shows the research objectives that the study is informed by.

1.1 Background and Importance of MOSFET Scaling

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the central component of electronic devices used today. Since their invention, transistors have gone through significant improvements in the form of the MOSFET and have found applications in microprocessors, memory chips, the Internet, and sensors and communications. The sheer scalability of these devices, Moore's Law has provided radical gains in the efficiency, speed, and transistor density in the last fifty years. [3] [6]

Historically, this scaling has been justified by such theories as Dennard Scaling, which ensured that the power density did not increase as device dimensions scaled down. The reduction of channel lengths and gate oxide thickness resulted in transistors that consume less power and switch faster, and therefore, portable and high-performance electronics were possible. However, as the ramping device geometry is scaled down to the nanoscale, conventional scaling approaches are becoming highly constrained. [4] [6]

1.2 Challenges in Advanced MOSFETs: Short-Channel Effects

Although scaling has resulted in tremendous advances in performance and integration density, its continued application was accompanied by several challenges. Short-channel effects (SCEs) become more

dominant in MOSFET behavior as the channel length scales towards 100 nm or shorter and lead to poor device electrical characteristics.

Key SCEs include

- **Drain-Induced Barrier Lowering (DIBL)** - lowering the barrier by the drain voltage, which decreases the threshold voltage.
- **Velocity Saturation** - when the velocity of the carrier drift attains a limit, no matter how high the electric field is.
- **Hot Carrier Effects** - this is a result of high-energy carriers that break down the gate oxide.
- **Oxide Charging and Ballistic Transport** - Charging in oxides, transport, and ballistic electricity transport at the deep nano-scale.

Such effects lead to the channel depth having less control by the gate, meanwhile adding to threshold voltage instability and higher leakage currents. The modern MOSFET design cannot, therefore, sustain a reliable performance as further scaling occurs. To be able to address them, a thorough knowledge of fundamental physics is needed, as well as the investigation of novel device architectures (silicon-on-insulator (SOI) and double-gate MOSFETs). [6] [17]

1.3 Role of Simulation Tools for Advanced Transistor Research

A correct modeling and simulation of MOSFET behaviour under varying conditions is required to learn and mitigate the limitations of short-channel effects. Nano-fabrication is expensive and time-consuming, prompting simulation as an important device development step.

Two major simulation tools can be observed within the framework of NanoHUB: the MOSFET Tool and the MUGFET (Multi-Gate FET) Tool, which are utilized in this thesis. They are both open-access online platforms that give a close look at the electrical properties of several transistor architectures.

MOSFET Tool can simulate bulk, SOI, and double-gate MOSFETs, and the user can:

- Modify critical physical parameters, including the channel length, the oxide thickness, and the doping concentrations.
- Note changes in current-voltage characteristics and threshold voltage.
- Compare long-channel and short-channel devices.
- Research on more advanced architectures such as SOI architectures and double-gate MOSFETs.[7]

The MUGFET Tool is used to simulate FINFET structure, which is becoming more popular in new nanoscale technologies. This tool allows:

- Analysis of 3D FINFET geometries with different fin widths and heights.
- Observation of threshold voltage behavior under aggressive channel length scaling.
- Comparison of FINFET performance with conventional devices in terms of electrostatic control and leakage suppression.

A combination of these tools offers a powerful simulation platform to investigate how physical and process parameters affect the performance of a device. These make it possible to study how architectural innovations, including multi-gate and FINFET designs, address the challenges of scaling. The knowledge of these simulations is used to aid academic exploration as well as industry-related optimization of next-generation transistor technologies.[5] [6] [9]

1.4 Aim of the Thesis

- To model and confirm the electrical behaviour of long-channel MOSFETs and FINFETS and compare with theory.
- To use the short-channel effects by steadily decreasing the channel length and comparing the way it would affect the threshold voltage and the device performance.
- To determine the sensitivity of critical design parameters-such as oxide thickness, channel doping, source/drain doping, substrate doping, and temperature, to the threshold voltage and transconductance.
- Compare advanced device architectures, including SOI, double-gate MOSFETs, and FINFETs, to conventional bulk MOSFETs with regard to the control of the threshold and short-channel immunity.
- To offer an insight into optimal design approaches in future high-performance, low-power nanoscale transistor technology.

2. LITERATURE SURVEY

Ongoing improvements in semiconductor technology have been substantially fueled by the incessant scaling of Transistor technology, which is the basic building block of electronics today. With the device dimensions reduced to the nanometer scale, the mechanisms of physical and electrical constraints of the transistors have gained greater significance in understanding and mitigating them. The effects of scaling on device performance have therefore been a hot issue among researchers who pay much attention to effects such as threshold voltage, leakage currents, and short-channel effects. To address those challenges, researchers are trying to develop new device architectures and more effective modeling methods. Simulation tools are also important, as they allow us to observe the behaviour of a device at varying designs and under varying environmental conditions. The literature review is a compilation of all the important theoretical and experimental studies that help us get where we are today in understanding how transistor works, and it helps shape more viable and scalable transistor technologies.

[6] is a textbook that explores deeply the physics, modelling, and scaling of MOSFETs in modern chips. It decomposes the behaviour of the standard bulk MOSFETs when devices are aggressively downscaled, highlighting the key limitations that emerge in the deep sub-micron and nanometer regimes. One of the debates it addresses is the emergence of short-channel effects (SCE), like a drain-induced barrier reduction (DIBL), roll-off of threshold voltage, and loss of mobility problems that severely affect reliability and switching speed. How to adjust the thickness of oxides, channel doping, and the gate length is also discussed by the authors to adjust electrical characteristics, including the threshold voltage and the sub-threshold swing. To add to that, Taur and Ning note changes to alternative device architectures such as SOI and double-gate MOSFETs, which they theorize and simulate are easier to electrostatically control and lower leakage. Their efforts support the analytical basis of the experimental simulation approach

employed in this thesis, and in particular with respect to visualizing the effects of parameter variations on device performance. The theoretical models of [6] can also be used to check the results of the simulation findings of NanoHUB that are used in this paper.

[1] offers a background knowledge of the physics underlying semiconductor devices, especially the electrostatics, carrier transport, and carrier behavior of p-n junctions and MOS structures. The text step-by-step explains the working of MOS capacitors and MOSFETs, and the derivation of the threshold voltage as a result of energy band diagrams and charge distributions in the oxide and substrate. The application of Pierret technology to modeling and simulation of MOSFET characteristics is particularly suitable, since the analysis structure presented is required to predict the effect of the various parameters of the device, including oxide thickness, doping concentrations, and channel dimensions, on threshold voltage and current-voltage characteristics. These principles serve as direct informants to the experimental studies carried out in this Thesis through the NanoHUB simulation platform. Another limitation of miniaturization of a device, which is also discussed in the textbook, is the insight into the impact of scaling on electric fields, leakage, and short-channel behavior, which is the key focus of interest behind studying advanced architectures such as SOI and multi-gate devices. In general, the work by Pierret can be viewed as the theoretical basis of the explanation of the baseline behavior of the long-channel MOSFETs as well as the degradation mechanisms that emerge during aggressive scaling.

[2] is a well-presented and easy-to-understand base of the functioning and design of semiconductor devices, in particular the MOSFETs. The book presents important physical concepts, namely carrier transport, energy band diagrams, and electrostatics of the MOS structure, in a manner that is more of a lecture note. It describes the dependence of the threshold voltage on the doping, the oxide thickness, and the geometry of the device, which I found crucial in coming to grips with actually understanding why a device acts the way it does. In addition to threshold voltage, Neamen goes into transconductance, or the

factor that informs us about the transistor's amplification of signals. It is evident in the text that transconductance depends on gate capacitance, carrier mobility, and channel length one thing that I pictured using those simple equations on my whiteboard. The author then connects these fundamentals to the simulation work in this thesis and demonstrates the behaviour of transconductance in various scaling conditions. It is as though you were to bridge theory and practice in a single paragraph. Neamen also addresses the short-channel effects and leakage that emerge in the shrink to nano-scale of devices, providing the groundwork to more advanced architectures like SOI and multi-gate transistors. Lastly, large- and small-scale behaviour are discussed, providing us with the context to balance performance trade-offs in scaled MOSFET design.

Literature Survey - Summary

The background that I have found in this literature review is a very solid one, and it really helps me to understand the effect on MOSFETs when you scale them aggressively. Taur and Ning, as well as Pierret and Neamen, give me an in-depth overview of the electrostatics, carrier transport, and design thinking I require to understand MOSFET performance. They all indicate how channel length, oxide thickness, and doping profiles influence physical parameters such as threshold voltage, leakage, and short-circuit effects. Even Taur and Ning consider higher-level architectures, including SOI and double-gate MOSFETs, which they claim can provide more control and reduced leakage. Pierret models allow me to model the behaviour of the transistor at the base, whereas the models provided by Neamen take a step further and introduce transconductance models and signal-performance models, which can prove the correct choice of the approach in this thesis and direct my research on the design of classic and innovative MOSFETs.

3. THEORY

The chapter discusses theoretical concepts that are the foundations of MOSFET operation, short-channel effects, and transconductance behaviour. It also presents more complex (advanced) transistor structures that include SOI and double-gate MOSFETs, FINFETs, which are to be examined in simulation analysis. These theories are critical to the interpretations of the results in this thesis and to the design trade-offs in scaling of transistor technologies. [1] [3]

3.1 Basic MOSFET Operation

The metal-oxide-semiconductor field-effect transistor (MOSFET) is a voltage-controlled device that acts as a current control passage through a semiconductor channel. It has four main terminals - gate, drain, source, and substrate (or body). The gate terminal adjusts to the flow of carriers (electrons or holes) between the source and drain through the applied electric field over the gate oxide.

In an n-type MOSFET (NMOS), when a positive voltage is applied with respect to the source at the gate, an inversion layer (n-channel) is created in the p-type substrate. Since it is always conducting when the mains voltage is applied across the drain, it allows current to flow from the drain to the source.[2]

Generally, there are three major regions of operation of MOSFETs:

- **Cut-off Region**: $V_{DS} = V_{GS} - V_t$, no conduction.

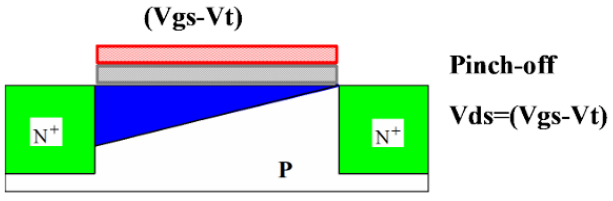

Figure 1. Cut-off Point

- **Linear Region**: $V_{GS} > V_t$ and $V_{DS} < V_{GS} - V_t$ channel behaves like a resistor.

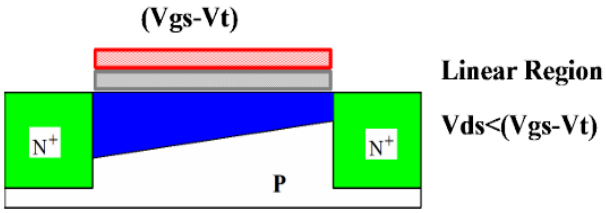

Figure 2. Linear Region

- **Saturation Region**: $V_{DS} > V_{GS} - V_t$, current independent of V_{DS}.

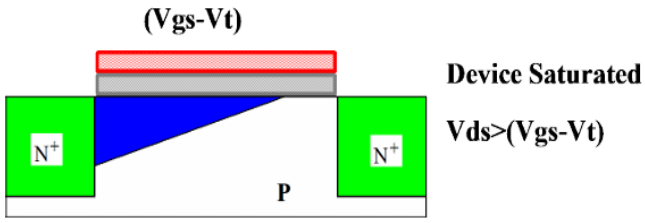

Figure 3. Saturation Region

Digital switching and analog amplification are based on these operating regions. [11]

3.2 Short-Channel Effects (SCEs)

Because the channel lengths of the MOSFET become nanometer-scale dimensions, as they diminish in size, the effects of short channels (SCEs) start to significantly change device performance. These effects occur when the length of the channel is of the same order as the depletion zones of the source and drain, resulting in loss of control by the gate over the channel potential.

Key SCEs are:

- **Drain Induced Barrier Lowering (DIBL)**: The drain voltage also drops the source-to-channel barrier and lowers V_t. Velocity Saturation: The carriers achieve a maximum drift velocity at high electric fields, and the current is thus limited.
- **Hot Carrier Effects**: High Carriers may also destroy the gate oxide or alter the threshold.
- **Threshold Voltage Roll-Off**: V_t also decreases as the channel length similarly minimizes along with the control of the gates.

Such effects were noticed in simulations in this study, especially at channel lengths smaller than 100 nm. The acquired results in the threshold voltage and transconductance were correspondent with the theoretical predictions about SCEs. [6] [17]

3.3 MOSFET Structures

Devices with smaller geometries need improved electrostatic control and short-channel effects suppressed, so alternative MOSFET structures have been invented to achieve this. This part describes three major MOSFET structures addressed by this thesis, namely Bulk MOSFET, SOI MOSFET, and Double-Gate MOSFET.

Bulk MOSFET (Planar MOSFET):

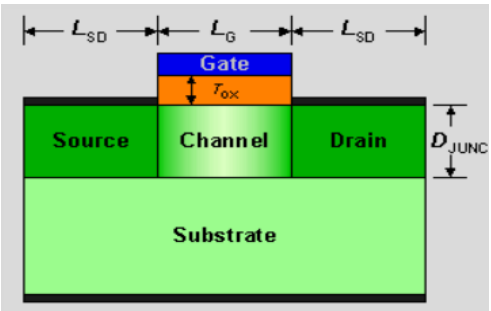

Figure 4.Bulk MOSFET

The most traditional and the most used structure of MOSFET is the bulk MOSFET. This is composed of a gate, source, drain, and a substrate (bulk) through which a current flows through the planar channel generated at the silicon surface.

Key features:

- Simple to make by conventional CMOS processes
- Low technology and inexpensive
- Still in widespread use until the sub-65-nm nodes in an integrated circuit

Limitations:

- Weakness in gate control in short-channel devices
- Significant Short-Channel-Effects such as Drain-Induced Barrier Lowering (DIBL)
- There is a high leakage current when the dimensions are small

Silicon- On- Insulator (SOI) MOSFET:

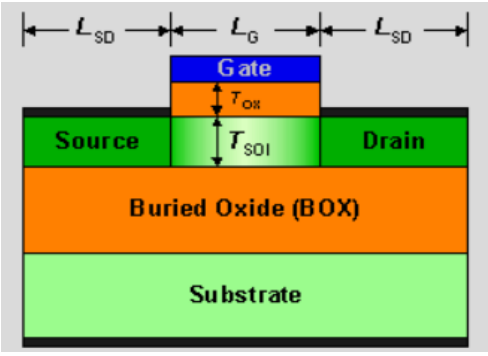

Figure 5. SOI MOSFET

SOI MOSFETs are made on a thin film of silicon, which lies on a buried oxide (BOX) layer to separate the transistor and the substrate. This minimizes parasitic capacitance and leakage.

Advantages:

- Small junction capacitance
- Improved subthreshold slope and switching speed
- Lower leakage current

Disadvantages:

- More costly because of special wafers
- Heat management - thermal problems because of ineffective heat dissipation (self-heating)
- Overall, SOI delivers a modest scaling as compared to bulk, but does not perform well at below 20nm nodes.

Double-Gate MOSFET:

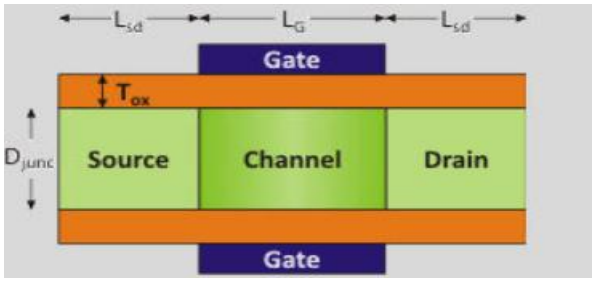

Figure 6. Double-Gate MOSFET

Double Gate MOSFETs are devices with two gates, which control the ambiance of a channel on both sides, bringing a huge gain to the electrostatic control over a channel.

Advantages:

- Better short-channel effect inhibition
- Reduced break voltage
- Greater drive current

Disadvantages:

- Complexity of fabrication (Exact gate alignment is required)
- Greater capacitance of the parasitics as compared to single-gate devices
- The transistors with double gates are more appropriate in aggressive scaling to 10-20nm. [16] [12]

3.4 Transconductance

The MOSFET transconductance is the ratio of the change in drain current to a change in gate voltage.

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

The transconductance is also called transistor gain.

In the case of an n-channel MOSFET in the non-saturation region, we have

$$g_{ml} = \frac{\partial I_D}{\partial V_{GS}} = \frac{W \mu_n C_{ox}}{L} V_{DS}$$

The transconductance varies directly with V_{DS} and does not vary relative to V_{GS} in the non-saturation area. The transconductance in this operating region is given by

$$g_{ml} = \frac{\partial I_D(sat)}{\partial V_{GS}} = \frac{W \mu_n C_{ox}}{L} (V_{GS} - V_T)$$

At the saturation region, the transconductance varies linearly with $V_{GS,}$ and it does not depend on V_{DS}. Transconductance depends on the device geometry and also on the carrier mobility as well besides the threshold voltage. Transconductance should rise with an increasing width of the device, and also rise as channel length and oxide thickness decrease. In MOSFET circuit design, transistor size, especially its channel width W, is an engineering design parameter. [1] [2] [6]

4. SOFTWARE TOOLS USED

4.1 MOSFET tool

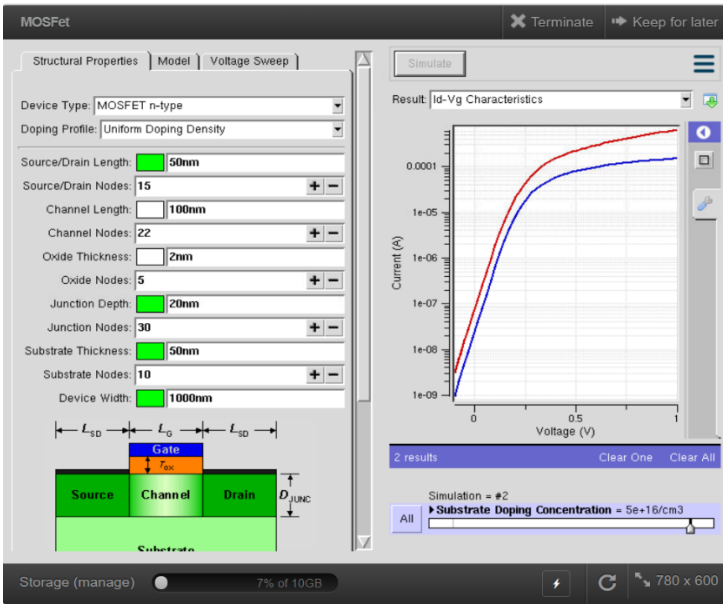

Figure 7. Overview of MOSFET Tool

In this work, the MOSFET Tool, which is found in NanoHUB, is taken as the main simulation platform to research the electrical behavior of MOSFETs in various conditions of scaling. The MOSFET Tool is a fairly useful, web-based simulation tool that allows us to have a look at how MOSFET design can be optimized by adjusting the most important variables, such as channel length, oxide thickness, doping levels, and operating voltages. It provides you with concrete information about the characteristics of devices, and it is a necessity when you are learning about the actual functioning of MOSFETs and you find that their operation could become flawed in certain circumstances, particularly short-channel effects. You can observe the behaviour of MOSFETs concerning I_D V_G characteristics, changes in threshold voltage, short circuit effects such as hot-carrier effects, velocity saturation, and oxide charge-up with the

tool. It also allows you to compare the devices in long channels with the smaller devices in short channels, to compare trade-offs between the two kinds in performance, and to test more complex designs of transistors, like double-gate MOSFETs and SIO technology.

It allows the user to model and analyze the electrical behaviour of an n-type MOSFET by adjusting the structural design and the level of doping. A user is able to set values of channel length, oxide thickness, doping concentrations, and junction depth to see their effects on important device properties such as threshold voltage and drain current.

The I_D V_G characteristics of the presented simulation are presented at two levels of substrate doping concentration, and the effect of doping on the flow of current and the threshold is also identified. The instrument is graphically displayed in real-time, which allows, in any case, the direct comparison of changes in parameters and is an efficient educational and research simulator of short-channel effects and scaling of devices in nanoscale MOSFETs. [9]

4.2 MUGFET Tool

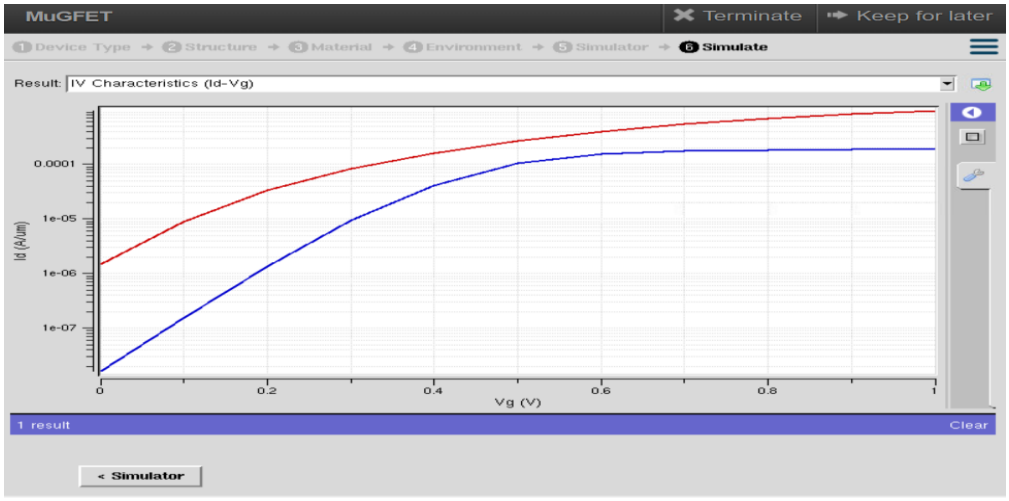

Figure 8. MUGFET Tool overview

The MUGFET Tool, which is found in NanoHUB, was used to simulate and analyze the behavior of FINFET structures under different scaling conditions. The simulation tool is created to investigate sophisticated transistor architectures that use more than one gate, like double-gate and FINFET transistors. Considering the increased relevance of FINFETs in nanoscale CMOS technologies, the MUGFET tool was a valuable resource to assess their electrical characteristics and electrostatic behavior.

The MUGFET tool has been used in this work to model the behaviour of FINFET workflows when we vary our design choices, particularly channel length, and see the impact of aggressive scaling on threshold voltage (V_t). Essential physical parameters like fin width, fin height, oxide thickness, and doping concentrations could also be customized, and we have the freedom to model realistic FINFET geometries. On the whole, the MUGFET tool helped analyze the performance of FINFET and may be an essential element in the development of low-power, high-performance transistors in the future.

It served as an addition to the MOSFET tool, providing more insight into the operation of multi-gate type devices and thus enhancing the analysis of the simulation-based analysis in this thesis. [11]

5. RESULTS

5.1 Baseline Device Parameters and Threshold Voltage

In order to explore how various design parameters work, we first built a default MOSFET model in NanoHUB with the MOSFET Tool. This initial setup is the reference point from which all the changes in parameters will be measured.

The table below presents the main physical and electrical parameters of the baseline setting:

Parameters	Values
Channel length	100 nm
Oxide Thickness	2 nm
Channel Doping Concentration	1 X 10^{18} cm^{-3}
Source/Drain Length	50 nm
Source/Drain Nodes	15
Junction Depth	20 nm
Temperature	300 K
Drain Current Target	10 µA

Table 1.Baseline Parameters

According to the parameters that we configured, the baseline voltage (V_t) was 0.21 V, which is in line with what you would expect of a long-channel bulk MOSFET operating under typical operating conditions.

This reference point provides us with a firm baseline by which we can determine the influence of various geometries, doping, and environmental changes on threshold voltage and overall performance.[1] [6]

5.2 Parameter Variation and Impact on Threshold Voltage

This section examines how variations in the design of significant design parameters influence threshold voltage (V_t) and the general behaviour of MOSFET devices using the MOSFET Tool. Adjustable parameters include channel length, channel, oxide thickness, and channel source, drain, and substrate

doping concentrations. These methodical variations enable us to know in detail how structural and material qualities influence switching behaviour and power efficiency.

In the assessment of these effects, this paper identifies significant design trade-offs, particularly scaling-based trade-offs such as short-channel effects. The results of the simulation are compared with the theoretical models to demonstrate the correctness of the results and suggest performance constraints and optimization techniques. Also, sophisticated device architecture, such as the use of double-gate FETs and SOI MOSFETs, is studied to assess their ability to address the challenges associated with scaling. [3] [6]

5.2.1 Influence of Channel Length on Threshold Voltage

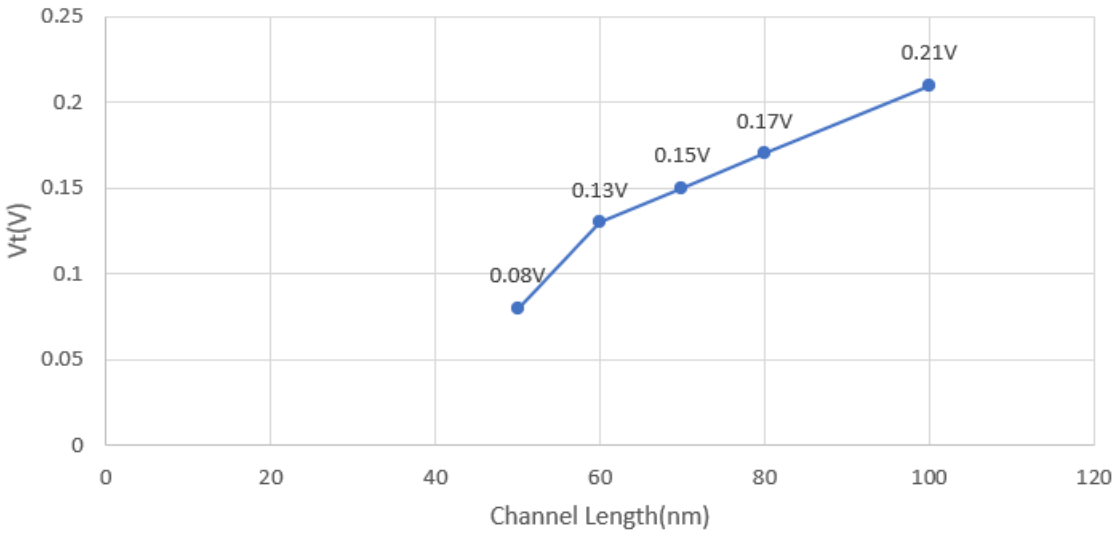

Figure 9. Observing V_t values altering Channel lengths (At 10 µA)

In Figure 9, the plot shows that when the length of the channel of a MOSFET shrinks from 100 nm to 50 nm, the value of the threshold voltage (V_t) also decreases from 0.21 V to 0.08 V. This effect is due to the so-called short-channel effects, which are more pronounced when device sizes decrease. In short-channel devices, the source and drain are located nearer to each other, and the gate is unable to completely control the channel. As a result, it becomes easier to influence the channel potential by the drain, and the transistor

can be turned on at a lower voltage. Among these principal sources of short-channel effects that cause such an effect is Drain-Induced Barrier Lowering (DIBL). Whereas the simple threshold voltage equation has no channel length terms, advanced models have a correction term to deal with this effect, which generally demonstrates that V_t can be reduced as the channel length gets shorter. This is why there is such a trend in the figure above, and this is what introduces the difficulties in making reliable transistors at such dimensions of the nanoscale. [6] [10]

The equation below shows the threshold voltage 'V_t' dependency on the channel length.

$$V_t(L) = V_{t_o} - \frac{C}{L^2}$$

Where:

- $V_t(L)$: Threshold voltage at a given channel length L
- V_{t_o}: Threshold voltage for a long-channel device (no short-channel effects)
- C: A constant that depends on the device and technology
- L: Channel Length

The equation shows that when L, the length of the channel, decreases, the value of $\frac{C}{L^2}$ increases, so when V_t is to be diminished, L must be reduced. This contributes to the fact that short-channel devices exhibit lower threshold voltages, as a result of a short-channel effect such as DIBL.

5.2.2 Influence of Oxide Thickness on Threshold Voltage

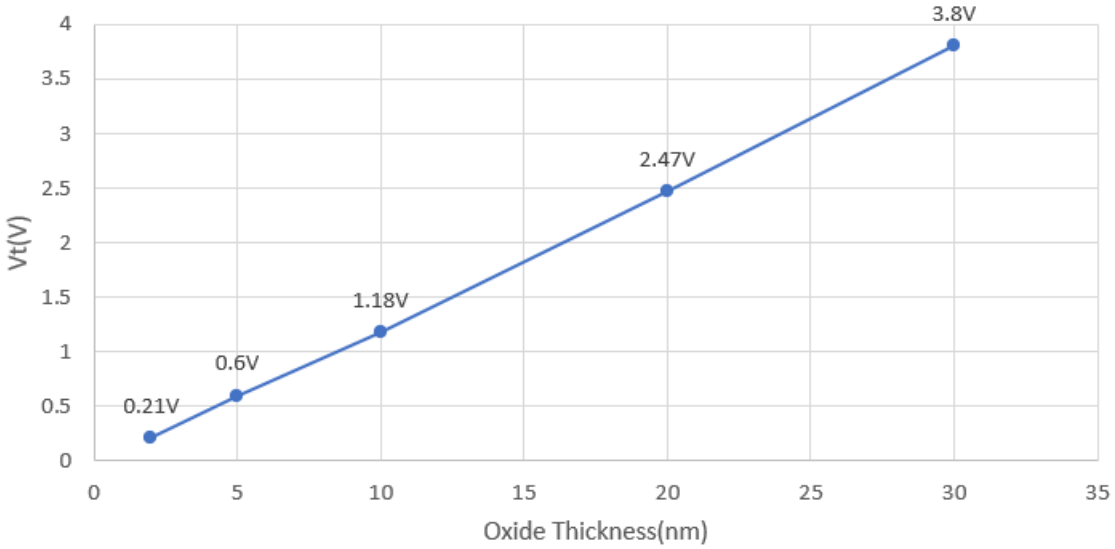

Figure 10. Altering T_{ox} and observing V_t (At 10 µA)

In Figure 10, the plot shows that as the oxide thickness (T_{ox}) becomes thinner from 30 nm to 2 nm, the threshold voltage (V_t) decreases from 3.8 V to 0.21 V. This occurs because a thinner oxide layer enhances the gate's control over the channel by increasing the electric field between the gate and the substrate. As a result, the transistor requires a lower gate voltage to turn on, leading to a reduced threshold voltage. This behavior is especially important in modern MOSFET designs, where scaling down T_{ox} is essential for faster switching speeds and lower power consumption. The basic relationship shows that V_t is directly proportional to T_{ox}, meaning that reducing the oxide thickness leads to a corresponding decrease in threshold voltage. [6] [8]

The dependency of the threshold voltage 'V_t' on the oxide thickness may be given by the equation below.

$$V_t = V_{t_0} + K \, . \, T_{ox}$$

Where:

- V_t: Threshold voltage
- V_{t_0}: Base threshold voltage
- T_{ox}: Oxide thickness.
- K: Constant

This equation shows that when T_{ox} is reduced, the added term becomes smaller, so V_t also becomes smaller.

5.2.3 Influence of Channel Doping on Threshold Voltage

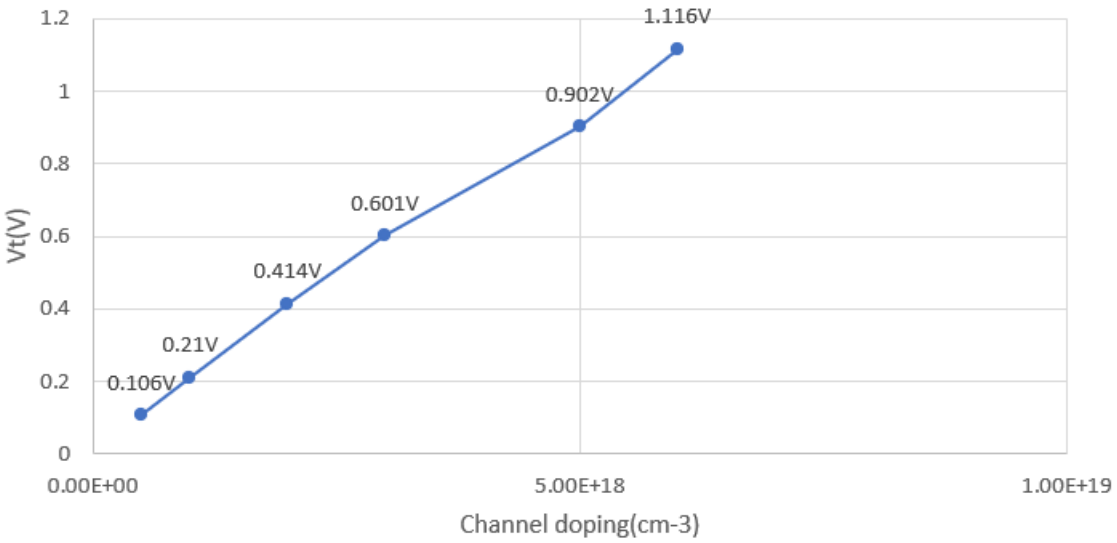

Figure 11. Observing V_t value altering Channel doping concentration (At 10 μA)

In Figure 11, the plot shows that as the channel doping concentration gets lower, the threshold voltage (V_t) will get lower. This is because the transistor is easier to turn on at a lower gate voltage due to low levels of doping, since the gate voltage can more easily invert the channel. The lower the number of atoms in the channel, the more easily the depletion region widens, and the electric field intensity needed to achieve inversion is reduced, leading to a lower threshold voltage. This is especially useful in

contemporary low-power MOSFET designs where the lower value of V_t has the benefit of faster switching speeds and lessening power consumption. In sum, the trend underscores the intuitive result that a decrease in the degree of channel doping results in an immediate reduction in threshold voltage that would be directly utilized toward performance optimization of advanced semiconductor devices. [1] [6]

The equation below shows the threshold voltage 'V_t' dependency on the channel doping concentration.

$$V_t = V_{t_0} + K\sqrt{N_A}$$

Doping concentration decrease: This equation demonstrates that this latest development brings down the doping level. N_A reduces the added term, and there is a smaller threshold voltage (V_t). The physical explanation of this is that there was less. N_A lowers the Fermi potential and the charge required to create the inversion layer, and as a result, the MOSFET can turn on at a low gate voltage. This means that less gate control is required to run the lower-doped devices, and this results in increased switching speed and decreased threshold voltage.

5.2.4 Influence of Source/Drain Doping Concentration on Threshold Voltage

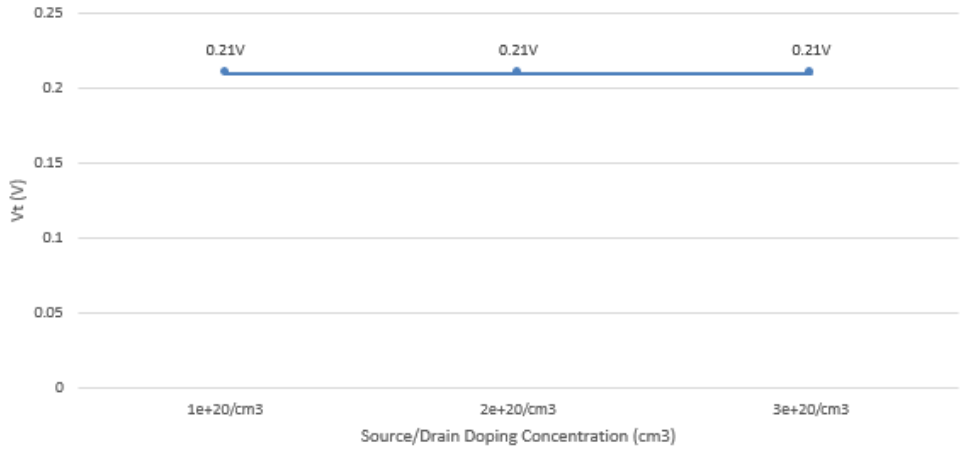

Figure 12. Observing V_t value altering Source/Drain doping concentration (At 10 µA)

In Figure 12, the plot shows that as the source/drain doping concentration reduces, the threshold voltage stays at 0.21 V. The drain and source areas in a MOSFET contain heavily doped elements, which ensure that their resistance is low and the injection of charge carriers into the channel takes place efficiently. These areas are physically isolated from the channel as a result of the melding together of the two junctions found at the source-channel and the drain-channel merge. The threshold voltage is mainly dependent on the charge actually required to turn the channel on, and to form a conductive path between the drain and source; changing source and drain doping makes no impact on this process.

- Making the source/ drain doping concentration larger increases current drive capability and minimizes series resistance, but does not change the threshold voltage since the inversion layer in the channel remains controlled by the gate voltage.
- The role of the heavily doped source and drain in the electric field that governs channel formation is regulated primarily by the gate-to-channel interaction.

Therefore, no matter what changes are made to either drain or source doping, the V_t will not change a great deal because these portions of the transistor are not contributing actively to the formation of the inversion layer. [1] [6] [13]

5.2.5 Influence of Substrate Doping Concentration on Threshold Voltage

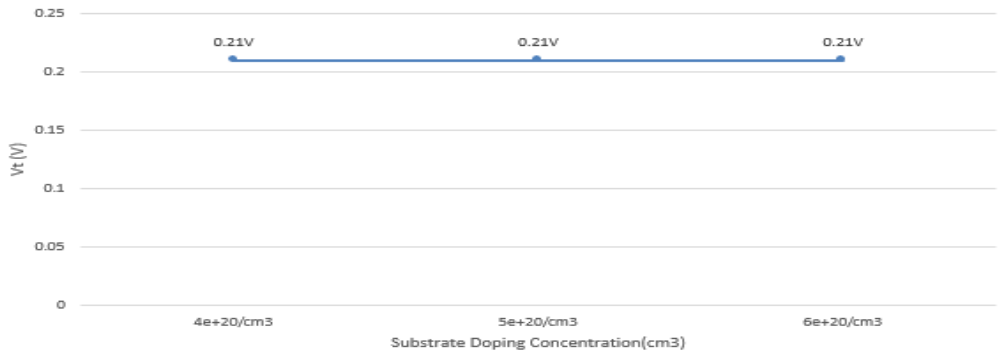

Figure 13. Observing V_t value altering Substrate doping concentration (At 10 µA)

In Figure 13, the plot shows that as the substrate doping concentration reduces, the threshold voltage stays at 0.21 V. The threshold voltage, however, is most commonly believed to be affected by the substrate (or bulk) doping concentration. Nevertheless, in contemporary MOSFETs, especially in simulation models where a highly idealistic environment is represented, the effects of substrate doping can be trivial on threshold voltage. [1] [6]

5.2.6 Influence of Temperature on Threshold Voltage

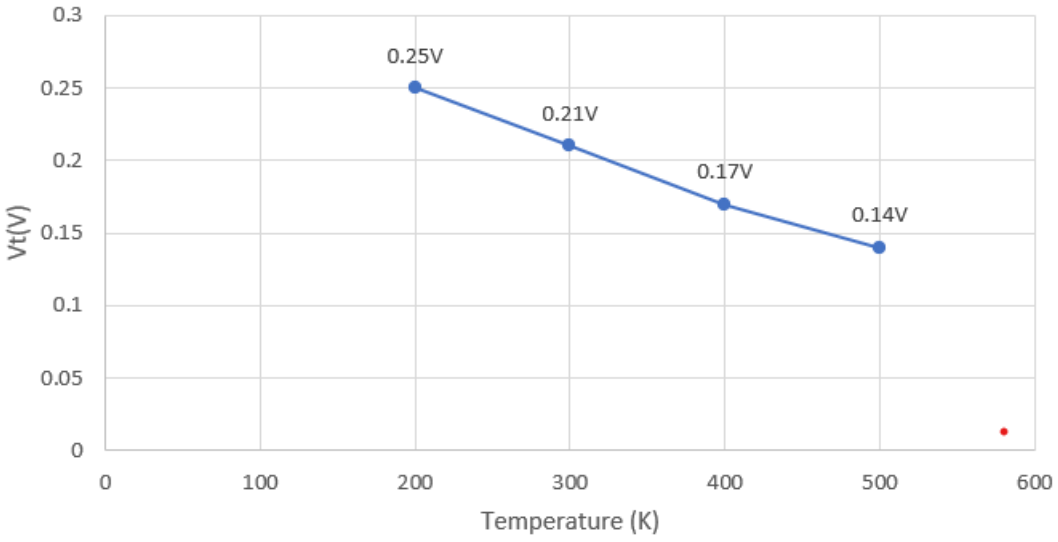

Figure 14. Observing V_t value altering Temperature (At 10 µA)

In Figure 14, the plot shows that as the temperature goes down, the threshold voltage (V_t) rises, as observed on the plot. It happens because at lower temperatures, the intrinsic carrier concentration of the semiconductor will dramatically drop. The decreased number of thermal carriers means the channel is more difficult to invert and thereby necessitating a higher gate electric field. This causes the MOSFET to have a higher voltage required to get into the on state, and this increases the threshold voltage. Also, the carrier mobility would be slightly enhanced at the lower operating temperatures, but the prevailing influence on V_t is the decreased availability of carriers to conduct. This trend is of particular interest in circuits where the devices can be subjected to different temperature environments. At low temperatures, where V_t is raised, slow switching, limited drive current, and/or failure to turn on (due to insufficient gate voltage) can occur. Thus, the knowledge of and compensation for temperature-dependent behavior plays a key role in achieving consistent operation of the MOSFET over various operating conditions. Described simply, for a reduction in temperature, the MOSFET requires a greater gate voltage to be conductive, hence a larger threshold voltage. [3] [6]

The equation below calculates the threshold voltage over a range of temperatures, 200 K to 500 K.

$$V_t(T) = V_{t_0} - \propto . (T - T_0)$$

Where:

- $V_t(T)$: Threshold voltage at temperature T
- V_{t_0}: Threshold voltage at a reference temperature T_0
- T: Current temperature
- T_0: Reference temperature
- $\propto$: Temperature coefficient

This equation shows that as temperature T decreases, the term $\propto .(T - T_0)$becomes more negative, so V_t increases as the temperature shrinks. It helps explain why MOSFETs require a higher gate voltage to turn on in colder conditions.

5.3 Baseline Configuration for Different MOSFET Devices

A simple set of physical and electrical parameters was simulated to provide a comparison of the behavior of various MOSFET architectures under identical conditions. This allows a variation in performance, e.g., a change in threshold voltage or transconductance to be present due to the device structure and not to different input parameters.

Parameters	MOSFET n-type	SOI n-type	Double Gate n-type
Channel length	100nm	100nm	100nm
Oxide Thickness	2nm	2nm	2nm
Channel Doping	1 X $10^{18}cm^{-3}$	1 X $10^{18}cm^{-3}$	1 X $10^{18}cm^{-3}$
Temperature	300K	300K	300K

Table 2.Baseline Parameter List of MOSFET Devices

The baseline configuration of the traditional Bulk MOSFET, Silicon-On-Insulator (SOI), and Double-Gate MOSFET devices that will be used in this work is presented in Table 2. Each of the simulations was carried out at a channel length of 100 nm, oxide thickness of 2 nm, channel doping concentration of $1\times10^{18}cm^{-3}$, and a temperature of 300 K. These standard parameters are used to make an equitable and consistent comparison of the electrical characteristics between architectures. [6] [12]

5.3.1 Threshold Voltage Comparison Across MOSFET Device Types

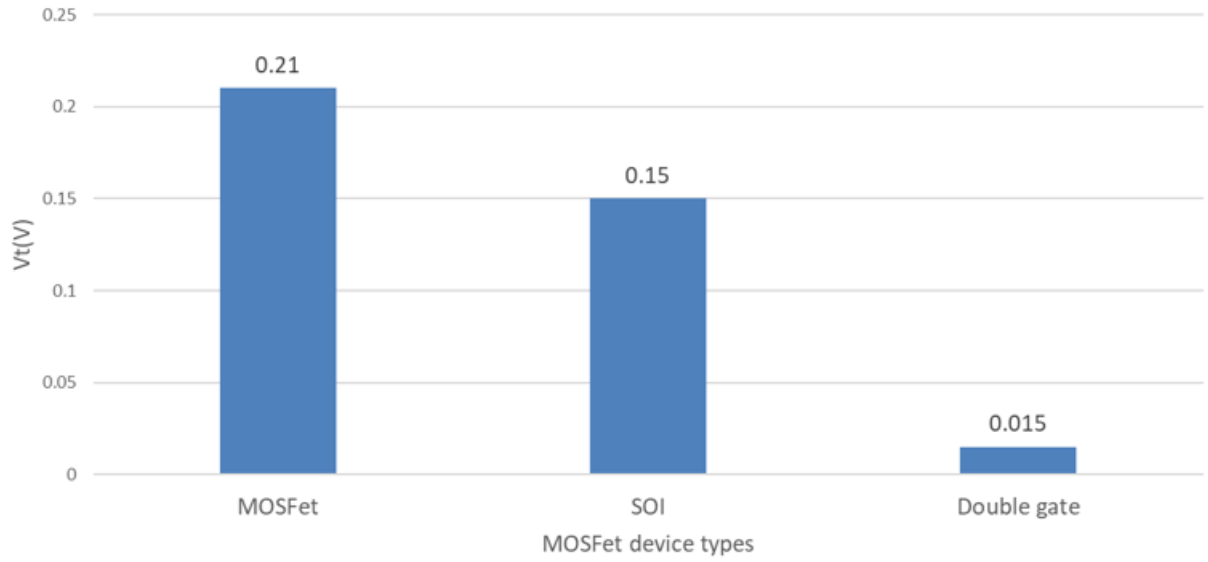

Figure 15. V_t values of MOSFET device types (At 10 µA)

Figure 15 indicates the difference in threshold voltage (V_t) of three types of Transistor devices. Conventional MOSFET, SOI (Silicon-On-Insulator), and Double Gate MOSFET. A conventional MOSFET has the highest threshold voltage (0.21V), SOI has moderate (0.15V), and the Double Gate MOSFET has the lowest V_t (0.015V). This is the case because advanced device structures demonstrate better Electrostatic control. In a bulk MOSFET, less precise gate control of the channel results in a large V_t and an amplified brief-channel impact. SOI technology mitigates these by adding a buried oxide layer, which enhances gate control that decreases its V_t relative to bulk. The Double Gate MOSFET goes further to use two gates to drive the channel on both ends, thereby greatly reducing leakage and increasing control to provide the lowest V_t. That means that double-gate structures will be suited to low-power, high-performance applications. [6] [14] [13]

5.3.2 Threshold Voltage Variation with Channel Length in MOSFET Devices

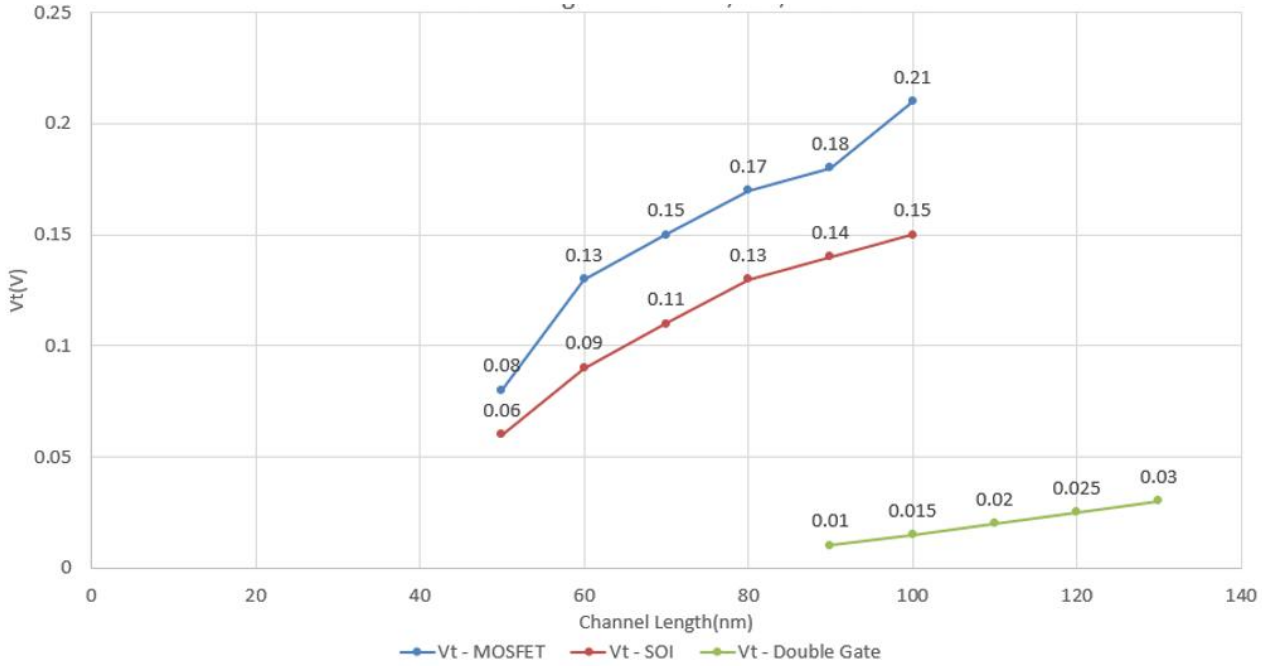

Figure 16. Channel length V_t variations

In Figure 16, the plot shows that as the channel length reduces, the V_t of all device types is reduced as the short-channel effects become more dominant, making the gate control on the channel less dominant. Traditional MOSFETs exhibit the largest V_t values due to inadequate electrostatic control and leading to high leakage at shorter lengths. Use of a buried oxide layer that in a way isolates the channel in SOI devices enhances their performance by minimizing leakage and lowering V_t than in bulk MOSFETs. The Double Gate MOSFET has the lowest V_t values with all channel lengths because the dual gate configuration ensures better channel control, which in essence counteracts the short-channel effects as well as leakage currents. This shows why advanced structures such as SOI and Double Gate MOSFETs have a scalability edge over their historical counterparts at nanoscales because of how advanced structures achieve lower V_t and improve with smaller geometries. [6]

5.3.3 Threshold Voltage Variation with Oxide Thickness in MOSFET Devices

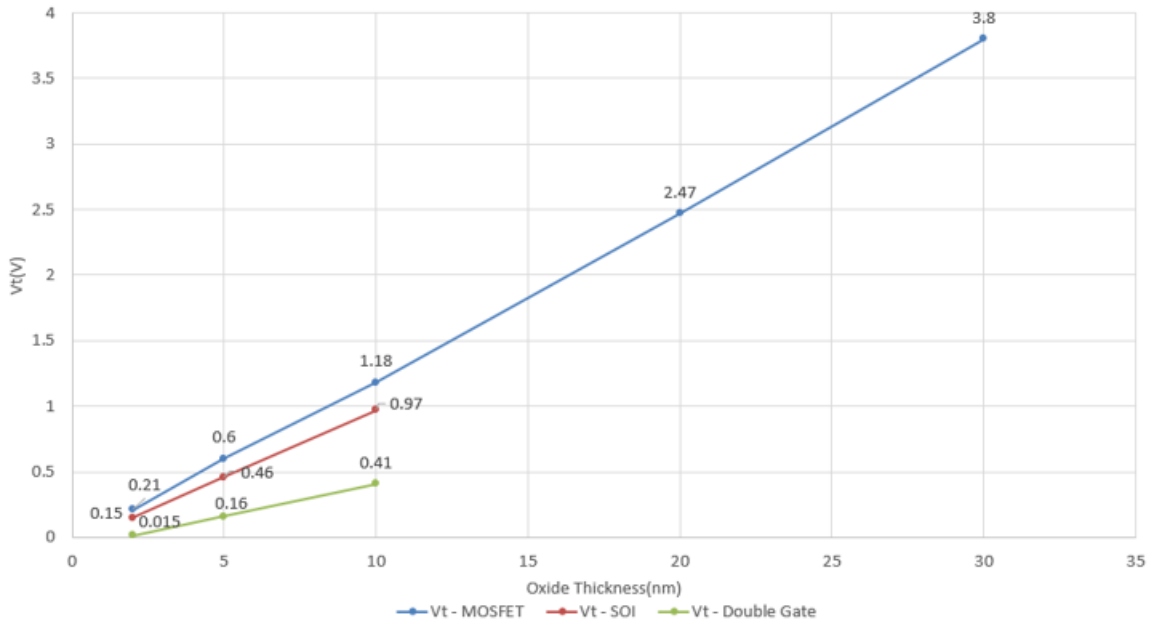

Figure 17. Oxide Thickness V_t variations

Figure 17 shows that all the device threshold voltage (V_t) decreases as the oxide thickness is reduced, and the conventional MOSFET experiences the largest fall in threshold voltage. This is because a thinner oxide layer increases gate control of the channel, so the device can turn on with a lower gate voltage. This change of a very sensitive nature to a bulk MOSFET device, as they are entirely dependent on the gate electric field to invert the channel via the oxide. The SOI (Silicon-On-Insulator) has an intermediate photon suppression.

The buried oxide layer already has a beneficial effect on electrostatic control, V_t, and so they are less sensitive to gate oxide thickness alone. The Double Gate MOSFETs offer the lowest V_t variations because their dual-gate structure offers optimum control over the channel that effectively reduces the effects of oxide thickness. This is among the reasons that advanced MOSFET structures have the benefit of sustaining consistent threshold behavior as oxide layers are aggressively reduced in the latest low-power and high-speed semiconductor processes. [6] [12]

The Double-Gate MOSFETs have much better electrostatic control than the conventional bulk and SOI devices because it has a dual-gate configuration, enclosing the silicon channel and effectively doubling the capacitance of the gate. This produces increased drive current and transconductance, allowing faster switching and better current delivery per volt of gate swing, even at extreme scaling to 50nm. The two-gate design greatly minimizes short-channel interactions, with a low threshold voltage (down to 15mV at 100nm) and enhanced stability under process, voltage, and temperature variations. In contrast to bulk devices with steep rises in V_t with oxide thickness, Double-Gate devices do not alter V_t and reflect their electrostatic strength. Moreover, they can maintain usable V_t and high-quality g_m even at high-temperature conditions, and therefore are very efficient in low-power, high-performance applications.[6] [12]

5.4 Variation of Transconductance with Channel Length in n-type MOSFET

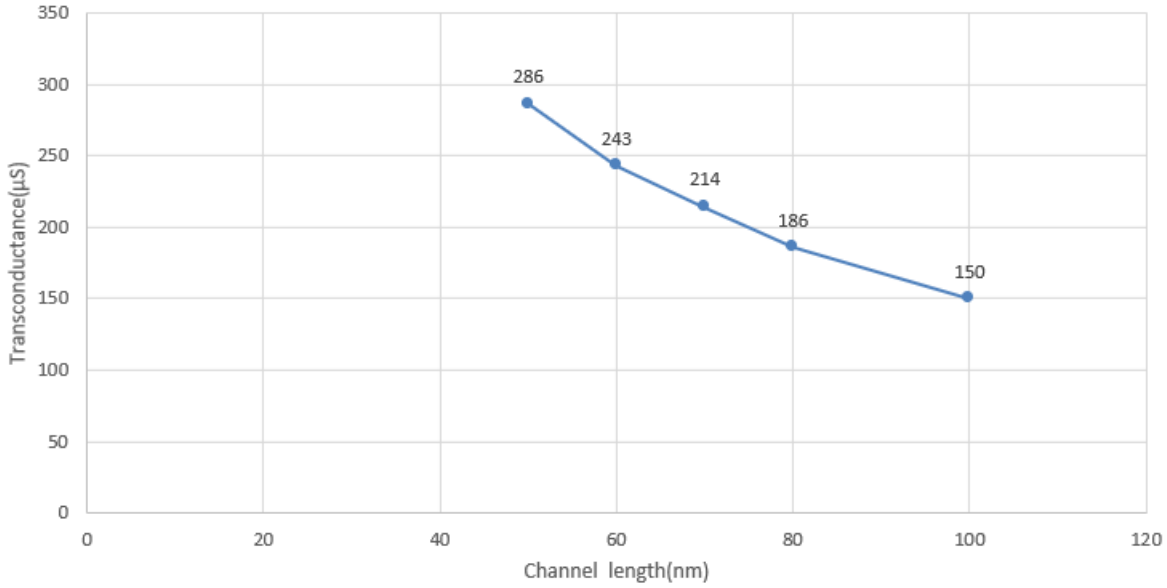

Figure 18. Transconductance variation

I extracted each g_m point by taking two nearby points on the same I_D–V_{GS} curve (measured at a fixed V_{DS} in saturation), reading off the drain currents I_1 and I_2 at gate biases V_{G1} and V_{G2} (with V_{G2}–V_{G1} kept small), and then computing

$$g_m = \frac{\Delta I_D}{\Delta V_G} = \frac{I_{D2} - I_{D1}}{V_{G2} - V_{G1}}$$

As the channel length decreases, the transconductance (g_m) of the n-type MOSFET rises considerably. The reason is that shorter channels have higher gate control over the channel; hence, the drain current can be modulated more strongly by a change in gate voltage. As shown in Figure 19, as compared to a 100-nm channel length, the current drive capability and stronger amplification are observed in the 50 nm channel length, which shows an increased transconductance. This is a great advantage of MOSFET scaling, given that the benefit, the smaller the dimensions, the better the performance. The shorter channel lengths provide both higher transconductance and speed, but they also present problems of short-channel effects and leakage currents. In general, the plot illustrates the inherent conflict in contemporary transistor design, that a smaller channel will offer better electrical performance but will need great control over other device parameters to remain stable and reliable. [1] [6]

5.4.1 Transconductance variation with channel length in MOSFET devices

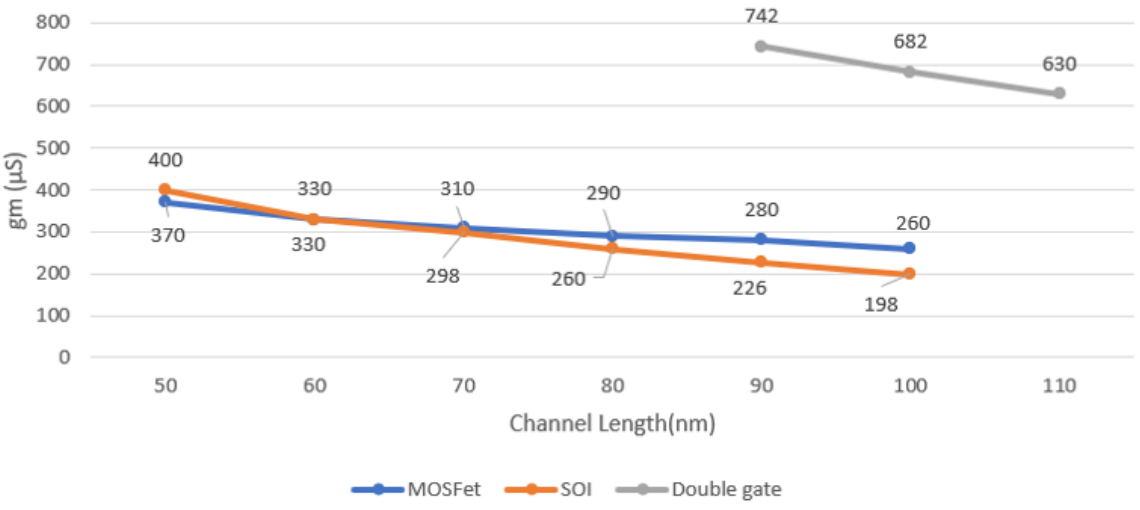

Figure 19. Transconductance variation with Channel length

The transconductance (g_m) of all MOSFET types of devices rises dramatically as the channel length is lowered. The reason is that shorter channels are less resistant between the source and the drain, hence,

more efficient carrier transport, and the channel is better controlled by the gate. A short channel length also increases the gate capacity to control the channel charge and creates a more notable drain current response to a change in the gate voltage. This causes an increase in g_m value, which is particularly desirable in analog and high-speed digital applications.

Out of the three types of devices under consideration, Bulk MOSFET, SOI, and Double-Gate, the Double-Gate MOSFET is the most notable in the trend of rising transconductance as channel length shrinks. At 50 nm, it has a g_m of 742 μS, and much greater than the respective values of SOI (400 μS) and Bulk MOSFET (370 μS). Such behavior can be attributed to the fact that the double-gate structure allows a more effective, electrostatic control of the channel, effectively raising the gate capacitance and allowing a better control of the carriers even in aggressively scaled devices.

With the SOI MOSFET, the reduction of channel size to 100 nm makes the g_m of 198 μS decrease to 400 μS. The enhancement is credited to less substrate effect and the decreased parasitic capacitance in SOI structures, which are more effective on smaller sizes. On the same note, the bulk MOSFET exhibits an increase in g_m of 260 μS at 100 nm to 370 μS at 50 nm. Nevertheless, the single gate and substrate coupling make it not scale as well as the other two architectures.

The plot confirms that channel-length shrinkage increases the transconductance; however, the extent of the increase is highly dependent upon the device architecture. Channel scaling is most favorable to multi-gate devices, especially double-gate MOSFETs, confirming their adoption in upcoming nanoscale and low-power device technologies. [1] [6] [12]

5.5 Channel Length Impact on FINFET Threshold Voltage

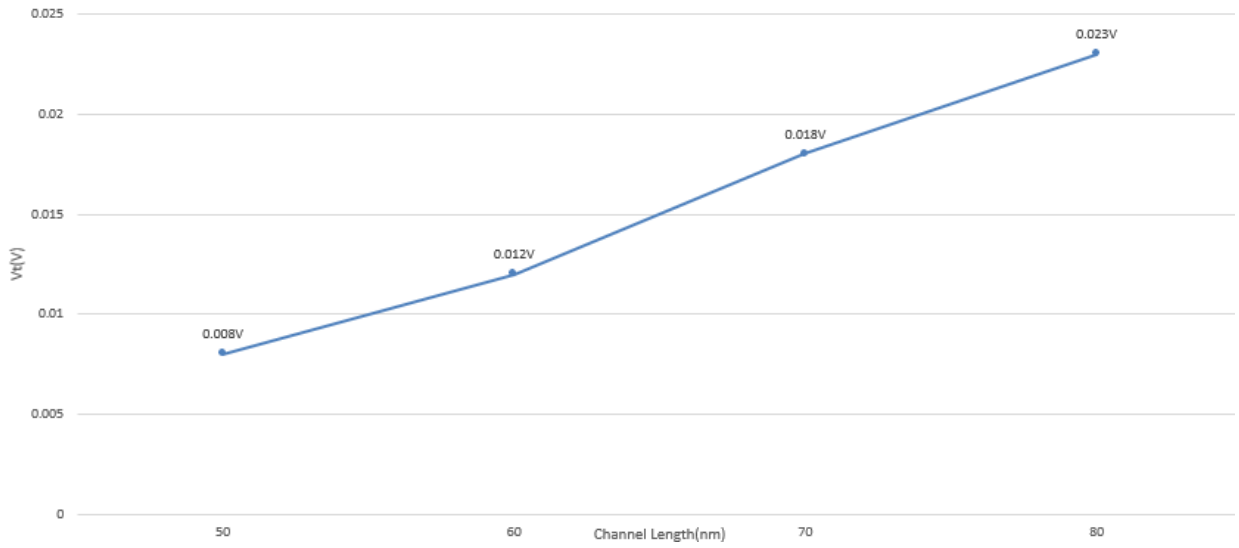

Figure 20. Threshold Voltage Variation with Channel Length for FINFET

The plot shows that the shorter the channel length of the FINFET device, the lower the threshold voltage (V_t). A reduction of the channel length by 80 nm to 50 nm means that the threshold voltage decreases by almost three times, to 0.023 V. This tendency proves that FINFETs, although their gate control is superior to that of planar MOSFETs, are indeed vulnerable to short-channel effects as their dimensions approach the nanoscale.

The reduction in channel length results in a decrease in the strength of the electrostatic control of the channel potential by the gate and enables the effects caused by the drain to reduce the barrier height and consequently V_t. This observation underscores the sensitivity of geometry optimization in the FINFET design to preserve confident switching properties in the next generation of nanoscale technologies.

5.5.1 Threshold voltage changes with channel length: FINFET vs. MOSFETs

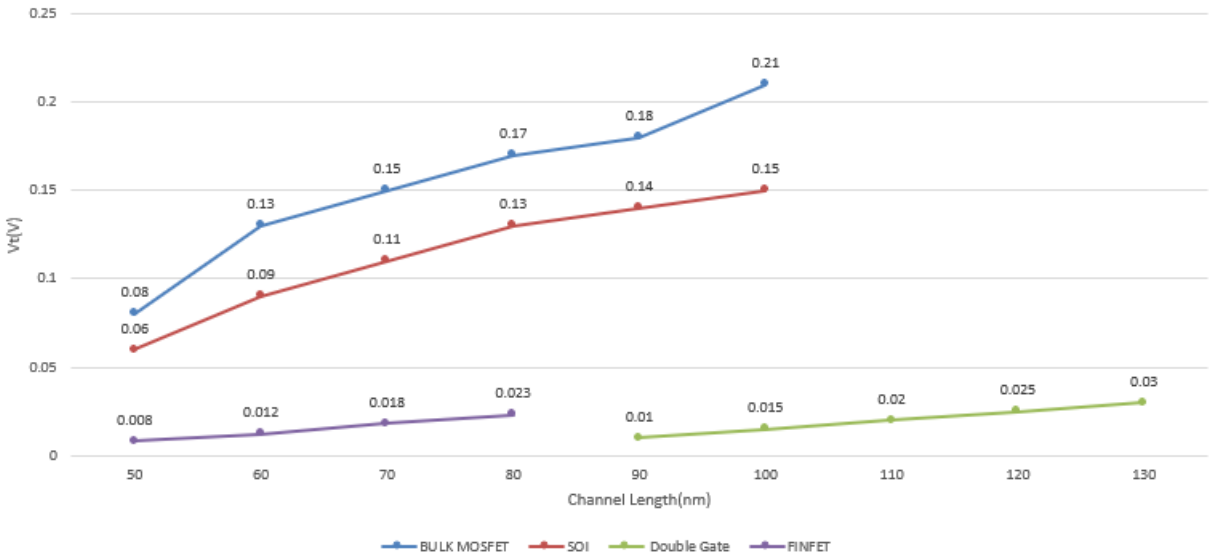

Figure 21. Threshold Voltage Variation across Transistors

The plot shows how the threshold voltage (V_t) varies with the channel length reduction in relation to the shrinking channel length of various MOSFET structures, namely the Bulk, SOI, Double Gate, and FINFET. The decreasing channel length causes a decrease in threshold voltage, which is more pronounced in all devices. Bulk MOSFETs are the steepest, falling between 0.21 V at 100nm to 0.08 V at 50nm, which means that short-channel effects are not well controlled. SOI MOSFETs are a little more effective, with better electrostatic control, but with a roll-off of the threshold. The data of the MOSFETs is restricted to longer channel lengths in the plot, as the Double Gate MOSFETs are more stable in V in a larger range of channel lengths. Contrastingly, FINFETs exhibit better aggressive scaling behavior, with threshold voltage increasing slowly as a function of gate length, 0.023, 0.008 V at 80nm and 50nm, respectively.

FINFETs have superior electrostatic integrity, reduced leakage, and more predictable behaviour, which makes them very promising in advanced nanoscale CMOS technologies. [15] [18] [19]

6. FUTURE WORK

Further research opportunities will remain beyond the field of this thesis as transistor scaling enters the deep nanometer regime. Although the present work has been able to establish the influence of the fundamental parameters of design on the threshold voltage and transconductance of various transistor-based architectures under varied conditions like channel length, oxide thickness, doping concentration, and temperature, it has left many gaps that need to be filled to understand the behavior of a device at the nanoscale in a more detailed way.

Even though FINFET results have been contained in this report, in future experiments, it is possible to extend the work to architectures working at sub-10 nm nodes. With the reduction of device sizes in size, the modeling in these sizes is critical to effectively determine short-channel effects and other quantum phenomena. Besides, the present work employed traditional SiO_2 as the gate dielectric, although the incorporation of high-k dielectrics like HfO_2 and metal gate stacks in subsequent models would be more reflective of industry trends. The benefit of these materials is higher gate capacitance and lower leakage, which is needed to further scale. We applied traditional SiO_2 as oxide scaling only in this work. We would like to experiment with high dielectrics like HfO_2 and metal gate stacks in the future to increase the gate capacitance, but without the undesirable leakages. That would keep us in the new CMOS trends. [20].

To those material-scale adjustments, we must take into account the non-idealities of the real world: mobility decreasing due to surface and impurity scattering, and interface traps that complicate things. It is indeed sensible to pass these effects on to later models, so that the simulated devices, in fact, resemble their performance when they are switched on and off.

The second summit thing that is promising is the application of machine learning to create predictive models by sifting through extensive simulation data. We can leave the computer to automatically optimize

design parameters, which is most convenient when we want to find the best settings in low-power or high-speed circuits.

Finally, we did a lot of simulations with NanoHUB, but it would have been very believable to the study if we were able to support the results with measurements in the real world of fabricated devices, or at least SPICE-level models based on the suppliers of real semiconductors. Simulation coupled with experimental data would not only reinforce our conclusions but also render the strategies that we are proposing more relevant to the industry.

7. CONCLUSION

The Thesis presented a comprehensive, simulation-based study of the behaviour of transistors under aggressive scaling, with special consideration to the behaviours of threshold voltage and transconductance with respect to changes in the structural and material parameters. The MOSFET, MUGFET tools of NanoHUB were used to systematically vary key design variables (channel length, oxide thickness, dopant levels, temperature), and their effect on device performance could be easily observed.

Important trends were detected through simulation. This reduction in channel length significantly influenced the channel length threshold voltage stability as the channel length had short-channel effects (SCEs), which increased leakage currents and decreased the reliability of the device. These issues were, however, resolved by other more recent structural approaches like Silicon-On-Insulator (SOI) and double-gate MOSFETs, which have better electrostatic control. Actually, FINFET designs, which were also investigated in this paper, demonstrated better threshold voltage characteristics and transconductance than standard planar devices. Although in some instances aggressive scaling may increase transconductance, it may also decrease performance unless structural improvements are made accordingly.

The semiconductor literature offered some theoretical models that provided a strong basis for the interpretation of the simulation results. This contribution fills the gaps between theory and practical modelling and adds to the overall effort to optimize transistor design for future low-power, high-performance devices.

Finally, the lessons Lastly, the research validates the usefulness of simulation to study modern devices and the need to adopt newer transistor architectures to continue scaling of performance to the nanometer order. The results and procedures mentioned herein are going to be helpful resources in further research in semiconductor device engineering and optimization of design.

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